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Using Miller's Theorem and Dominant Poles to Accurately Determine Field Effect Transistor and Bipolar Junction Transistor Small Signal and SPICE Capacitor Values

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Abstract

The most accurate method for determining high-frequency cutoff for Bipolar Junction Transistor (BJT) and Field Effect Transistor (FET) small-signal amplifiers is to use Miller's Theorem to simplify frequency response analysis. Dominant pole analysis can be used to further simplify calculations of the high-frequency cutoff. Unfortunately, accurate small-signal capacitance values are difficult to determine. Using manufacturer's SPICE data for these values can yield large errors when comparing simulation, analysis and experimental data.

This paper proposes a new technique consisting of several simple measurements to determine the intrinsic capacitances of transistors. The technique uses dominant pole analysis under two different signal source resistance conditions. Two different dominant poles result: a dominant pole due to low signal source resistance and another for a high signal source resistance. The dominant pole due to the high source resistance is associated with the equivalent input capacitance pole of the high signal source resistance transistor amplifier. The dominant pole corresponding to the low signal source resistance is associated with the equivalent output capacitance pole of the low signal source resistance transistor amplifier.

Accurate small signal (e.g. hybrid-π) capacitance values are determined by experimentally determining the two high-frequency cutoff frequencies (dominant poles) from the two signal source resistance conditions using essentially the same basic amplifier, and through analytic expressions for the two poles of the small-signal amplifier model. These values are mathematically converted to SPICE equivalent transistor model capacitances using established SPICE relationships. SPICE simulation using these values corresponds well with experimental data and analytic calculations.

Students in junior- and senior-level electrical engineering electronics courses at the University of San Diego (USD) performed an exercise, including both simulation and experiment, using this technique. Assessments of the student gains in knowledge and confidence in applying the dominant pole calculations to determine transistor model capacitances and in the design of other active circuits using this method are on-going. Faculty assessment of student results and gains in confidence, as measured by scoring short answers to knowledge statements, will be presented.

I. Introduction

Accurate determination of intrinsic Bipolar Junction Transistor (BJT) and Field Effect Transistors (FET) capacitances in the small-signal equivalent circuit models of transistors is important for the design and simulation of amplifier in electrical engineering electronics courses. Correspondence of computer simulations using standard manufacturer models for FETs and BJTs do not typically match experimental verification of amplifiers using those models. Several

methods have been proposed for measuring these parameters[1,2]. Unfortunately, some methods propose etching materials from a semiconductor structure.

This paper proposes a new technique consisting of several simple measurements to determine the intrinsic capacitances of transistors. Using measurements from these test circuits, good approximations of the intrinsic capacitances of BJTs and FETs can be determined and used in computer simulations and calculations.

The proposed technique uses the well-understood dominant pole method to measure the bandwidth of a transistor circuit and using that bandwidth to back-calculate the intrinsic transistor capacitances. The advantage of this method is that a specially fabricated test structures are not required and simple data processing of measured bandwidth is used to perform a simple calculation of intrinsic capacitances of the BJT hybrid-π model C_π (base-emitter capacitance) and C_μ (base-collector capacitance), and FET small signal model C_{gs} (gate-source capacitance) and C_{gd} (gate-drain capacitance).

II. Proposed Method and Measurements

Standard small-signal high frequency models of BJTs and FETs are used. The models used are shown in Figure 1.

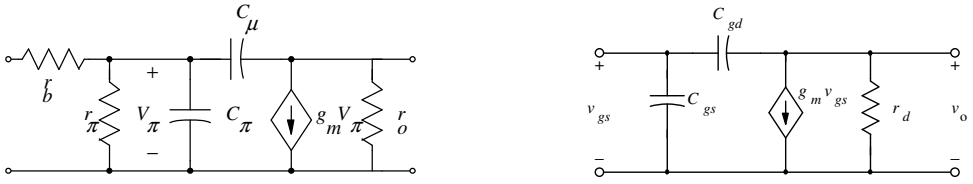

Figure 1. (a) BJT small signal hybrid-π model (b) FET small signal model

To accurately simulate transistor amplifier frequency response, good approximations of the intrinsic BJT capacitances C_π and C_μ, and FET capacitances C_{gs} and C_{gd} must be obtained. In order to evaluate and use C_μ and C_{gd}, Miller's theorem must be used in conjunction with measured dominant pole voltage gain and bandwidth measurements.

Miller's Theorem has become a standard tool in the analysis of the high-frequency behavior of transistor amplifiers. In particular, Miller's Theorem is useful in cases where a circuit element bridges the input and output terminals (C_μ or C_{gd} for this method). In these cases, a bridging capacitor is converted into two equivalent capacitors that shunt the input and output terminals (Figure 2). The transformation of a bridging capacitor, C, to its equivalent input capacitance, C_1, and output capacitance, C_2, is given by:

$$C_1 = C(1 - A) \qquad C_2 = \frac{(A-1)C}{A}$$

There are, unfortunately, some problems associated with the application of Miller's Theorem to transistor amplifiers, primarily in that Miller's Theorem requires a voltage-gain model, while most transistor amplifier models (in particular, the common-emitter amplifier) lead to a

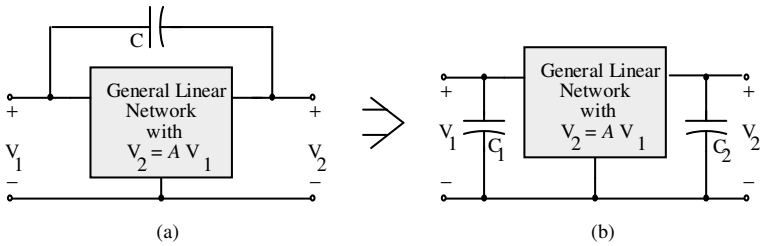

Figure 2 Miller Equivalent Circuits

transconductance model as a direct result of the small-signal transistor models (Figure 1). In addition, most calculations are based on the midband voltage gain of the amplifier, where Miller's Theorem does not utilize that restriction. Nonetheless, reasonable approximations can be made. Typical expressions for the poles of a common-emitter amplifier are shown in Table I and are essentially those found in many electronics textbooks. All equations have been rewritten to eliminate notation inconsistencies. Table II provides similar pole frequency equations for common-source FET amplifiers.

Table I. Summary of BJT common-emitter pole frequencies

Pole	Pole Frequencies
A	$\omega_{HA} = \dfrac{1}{R_i\left\{C_\pi + \left(1 + g_m R_o\right) C_\mu\right\}}$
B	$\omega_{HB} = \dfrac{1}{\left\{1/g_m + R_o\right\} C_\mu}$

Table II. Summary of FET common-source pole frequencies.

Pole	Pole Frequencies
A	$\omega_{HA} \approx \dfrac{1}{R_i\left\{C_\pi + \left(1 + g_m R_o\right) C_\mu\right\} + R_o\left(C_\mu + C_L\right)}$
B	$\omega_{HB} \approx \dfrac{1}{\left\{1/g_m + R_o\right\} C_\mu + C_L R_o}$

In nearly all common-emitter or common-source amplifiers, one pole is dominant and the high 3-dB frequency is essentially the lower of the two pole frequencies. It is important to note that many electronics textbooks list only the Miller effect pole (ω_{HA}) and have thereby predetermined that the Miller effect pole is always the dominant pole. As shown in this paper and in Schubert and Kim[3], the Miller effect pole is not always the dominant pole.

Of particular significance is, in both the BJT and FET case, that pole A (as described ω_{HA}) is

highly dependent on the output resistance of the signal source, R_i, while pole B (as described ω_{HB}) is independent of the signal source output impedance. That dependence-independence relationship of the poles is such that pole A is dominant for large signal source output resistance and pole B is dominant for small signal source output resistance.

The method described in this paper takes advantage of the switching of dominant poles with signal source output resistance in order to easily calculate the transistor model capacitances, C_π and C_μ, by merely measuring the high 3-dB frequency of a single amplifier driven by two different signal sources: one with a low output resistance (typically the 50Ω output resistance of a function generator), and one with a resistor inserted between the signal source and the amplifier. C_μ can be directly computed from the high 3-dB frequency for the low output resistance case and, using that value of C_μ, C_π can then be computed from the high 3-dB frequency for the high output resistance case. In this paper, MathCAD is used to find those transistor intrinsic capacitance values. Once the intrinsic capacitance values are calculated from the measured dominant pole test circuits, SPICE models are back-calculated using the standard expressions for converting small-signal model capacitances to capacitances used in the SPICE models (Table III).

Table III. BJT and FET Intrinsic Capacitance Conversion Equations from SPICE Model Capacitances

Transistor Type	Spice Model Parameter
BJT	$C_\mu = \dfrac{CJC}{\left(1-\dfrac{V_{be}}{VJC}\right)^{MJC}}$ $C_\pi = g_m TF + \dfrac{CJE}{(1-FC)^{1+MJE}}\left[1-FC(1+MJE)+MJE\dfrac{V_{be}}{VJE}\right]$
FET	$C_\mu = C_{gd} = \dfrac{CGD}{\left(1+\dfrac{\lvert V_{GD}\rvert}{PB}\right)^{M}}$ $C_\pi = C_{gs} = \dfrac{CGS}{\left(1+\dfrac{\lvert V_{GS}\rvert}{PB}\right)^{M}}$.

The method used to determine the transistor intrinsic capacitances is:

1. Design a common emitter amplifier (BJT) or common source amplifier (FET) and measure the BJT collector current and base-emitter voltage, or the FET drain current, gate-to-drain voltage and gate-to-source voltage.
2. Determine the small signal voltage gain of the amplifiers
3. Using the small-signal voltage measurement, determine the transconductance, g_m, from Table IV.

4. Measure the dominant pole (high cut-off frequency) response for high signal source resistance.
5. Measure the dominant pole response for low signal source resistance.
6. Using the equivalent input and output capacitances, determine the intrinsic small signal hybrid-π capacitances, C_π and C_μ, or FET small signal capacitances, C_{gs} and C_{gd}.
7. From the calculated small signal capacitances and previously measured values, determine the SPICE model capacitances using Table III.

Table IV. Transistor transconductance, g_m equations

Transistor Type	Transconductance g_m
BJT	$g_m = \frac{h_{fe}}{r_\pi} = \left\lvert \frac{I_C}{\eta V_t} \right\rvert$
JFET and Depletion MOSFET	$g_m = \frac{2I_D}{V_{GS} - V_{PO}} = 2\sqrt{I_D \frac{I_{DSS}}{V_{PO}{}^2}}$
Enhancement MOSFET	$g_m = \frac{2I_D}{V_{GS} - V_T} = 2K(V_{GS} - V_T) = 2\sqrt{I_D K}$

III. Example Determination of SPICE Capacitance Parameters

As an example of the method described above, the SPICE capacitance parameters CGD and CGS will be determined from pseudo-experimental (simulation) results for a given JFET (arbitrarily chosen as 2N5486). Electrical engineering students at USD have previously had experience in the determination of low-frequency SPICE parameters. For JFETs, a transistor curve tracer is used to find the parameters V_P and I_{DSS} from which the SPICE parameters VTO and BETA are obtained using typical expressions. For this simulation example, the manufacturer's SPICE parameters (VTO = −3.847 and BETA = 8.32666e-4) will be used rather than actual experimental data.

The transistor is then biased into the saturation region (forward-active region if a BJT) as a common-source amplifier (common-emitter for a BJT). The high 3-dB frequency of that amplifier is determined under two signal source conditions: high and low signal source output impedance (Figure 3). The data from the two experiments is tabulated in Table V. Note that it is important that the poles be dominant poles: the signal source output resistances must be chosen so that the high 3-dB frequencies differ by at least a factor of four.

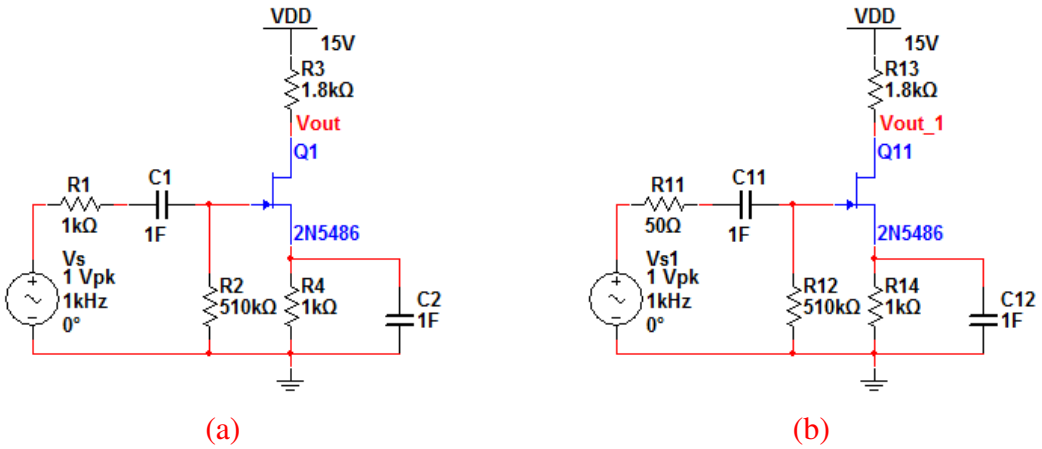

Figure 3. Two high frequency 3-dB test circuits:
(a) High signal source output resistance
(b) Low signal source output resistance

Table V. Results from the tests of Figure 3

Parameter	**Experimental Value**
Midband voltage gain	**–4.936**
Drain current	**2.29 mA**
V_{gs}	**–2.29 V**
V_{gd}	**–10.9 V**
High R high 3-dB freq.	**21.0 MHz**
Low R high 3-dB freq.	**98.86 MHz**

Sample MathCAD calculations are shown in Figure 4. Here, as would be usual for an unknown transistor, typical values for the SPICE parameters PB, the gate *p-n* potential, and M, the gate grading coefficient, are used. SPICE simulation using the newly-calculated SPICE parameters results in a high 3-dB frequency of 19.0 MHz (-9.5% or -.044 decade) when applied to the high signal source resistance case and 107.6 MHz (+8.8% or +0.038 decade) when applied to the low signal source resistance case. The authors consider the high 3-dB frequency match to be excellent: much better than the typical match between experiment and simulation.

Determination of Miller's Capacitances for FETs

Measure ID, Vgs, and Vgd --- measure the voltage gain Av -- enter results of measurement below

$I_D := 2.29 \cdot 10^{-3}$ $V_{gs} := -2.29$ $V_{gd} := -10.9$ $Av := -4.936$

Enter the Drain resistor value, the 2 signal source resistances, and the load capacitance (if any):

$R_D := 1800$ $R_{HS} := 1000$ $R_{LS} := 50$ $C_L := 0$

Determine the FET small-signal transconductance:

$$g_m := \frac{-Av}{R_D} = 2.742 \times 10^{-3}$$

Enter the experimenal high 3-dB frequencies for each source resistance case:

$f_{HighR} := 21 \cdot 10^6$ $f_{LowR} := 98.9 \cdot 10^6$

The equations below determine the FET analytic model

$$C_\mu := \left[\frac{1}{\left(\frac{1}{g_m} + R_D\right) \cdot 2\pi \cdot f_{LowR}} - \frac{C_L \cdot R_D}{\left(\frac{1}{g_m} + R_D\right)} \right] = 743.417 \times 10^{-15}$$

$$C_\pi := \frac{1}{2\pi f_{HighR} \cdot R_{HS}} - \left(1 + g_m \cdot R_D\right) \cdot C_\mu = 3.166 \times 10^{-12}$$

The equations below determins the FET SPICE model capacitances
(SPICE typical values are M = 0.5 and PB = 0.6):

$M := .5$ $PB := 0.6$

$$CGD := C_\mu \cdot \left(1 + \frac{|V_{gd}|}{PB}\right)^M = 3.255 \times 10^{-12} \qquad CGS := C_\pi \cdot \left(1 + \frac{|V_{gs}|}{PB}\right)^M = 6.948 \times 10^{-12}$$

Enter the values into the FET model in SPICE

Figure 4 Sample MathCAD calculations of SPICE capacitance values

IV. Assessment

In the fall semester of 2012, 15 students performed a laboratory exercise using these methods. Preliminary student assessment of experimental and simulation data shows results consistent with the finding of this paper. A detailed assessment will be made available upon gathering a larger sample size. In the spring semester of 2013, an additional 20 students will perform the same laboratory exercise.

One of the aims of this study was to assess student learning in laboratory concerning design and simulation of transistor circuits. Specifically:

- Does this design methodology increase basic understanding of transistor amplifier and design tools?

- Does student confidence in applying the concepts learned and using PCB design tool increase?

Short questionnaires were designed to provide insight into the student level of knowledge concerning the design and analysis of amplifier circuits and their confidence in applying that material. At the beginning of the design exercise, students were asked to score (on a scale from 1 to 5) their prior knowledge. To provide further insight into actual student knowledge level, students were asked to respond with a short answer to the knowledge questions, and these short answers were scored by the investigators at a later time. After the design exercise was completed, the questionnaires were again completed by the students and the post-exercise written responses scored by the investigators to measure changes in knowledge level. In order to track individual student incremental changes, each survey was coded with a secret number, thereby preserving student anonymity. The use of student-assigned scores to assess gains in student knowledge and confidence has been successfully used by the investigator team in previous studies by Schubert, et. al.[4, 5] .

The following eight questions concerning knowledge concerning transistor capacitance modeling were asked before and after the lab exercise:

1. What are the capacitors used in the high-frequency small-signal model of Bipolar Junction Transistors (BJT)?
2. What are the capacitors used in the high-frequency small-signal model of Field Effect Transistors (FET)?
3. How do you determine the small-signal model capacitors for a particular transistor?
4. How is Miller's Theorem used (in words) for transistor amplifier high-frequency small-signal models?
5. What is a dominant pole (high frequency)?
6. What are the primary factors affecting a dominant pole?
7. In a transistor amplifier, what are some of the major factors contributing to mismatches between analytic and computer simulation results?

The knowledge score was based on the following scale:

1 = No clue, this concept is new to me
2 = Low, I have only heard about the concept
3 = Moderate, I know about the concept, but have not applied it
4 = High, I know the concept and have tried it
5 = Superb, I know the concept and have successfully applied it

The distribution of students' answers on their knowledge of intrinsic transistor capacitance design concepts and practice before and after the exercise will be provided at the conference when a significant data sample is achieved in Spring 2013 . Preliminary results of the student survey showed student calculated and simulated high cut-off frequencies consistency between the SPICE and measured results within approximately 10%.

Students reported initial knowledge of intrinsic transistor capacitance design of a mean = 3.2 (moderate), reporting changes in mean scores due to the lab exercise +0.8 change (high knowledge). The mean knowledge level increased for each question at or above 0.70 with the questions relating to transistor capacitance experiencing the greatest mean difference +1.05. Faculty scoring of the student short responses to the initial knowledge statements showed good correlation with student reporting of knowledge of a mean score of 3.3. Faculty scored a somewhat smaller overall mean knowledge increase of 0.5.

Another portion of the questionnaire was designed to assess student confidence in applying the concepts of the design process. The following nine questions were asked before and after the exercise were performed in order to assess student confidence:

1. I can design transistor amplifier circuits.
2. I can apply Miller's Theorem to create small signal models of electronic circuits.
3. I can perform high-frequency small-signal analysis of analog electronic circuits
4. I can determine circuit high-frequency dominant poles.
5. I can use computer simulation tools for analyzing electronic circuits.
6. I can convert between the transistor parameters used in analytic models and those used in circuit simulation models
7. I can compare high-frequency cut-off calculations for transistor amplifiers circuits and verify performance characteristics using computer simulation
8. I can reconcile mismatches between analytic and simulation high-frequency cut-off results

The confidence score was based on the following scale:

1 = No Clue, I have no idea if I can apply the concept
2 = Low, I have heard of the concept, but have little confidence that I can apply it
3 = Moderate, I think I understand the concept, but am unsure about applying it.
4 = High, I am fairly sure I understand the concept and am fairly sure I can apply it.
5 = Superb, I am very confident that I understand the concept and can apply it to a new problem

The detailed distribution of students' answers on their confidence in applying intrinsic transistor capacitance design concepts and practice before and after the exercise will be provided at the conference when a significant data sample is achieved in Spring 2013. Preliminary results showed student knowledge and confidence score increased by about 1.2 after the exercise was completed.

Students reported higher initial confidence in topics relating to transistor amplifier design questions 1, 3, and 5 (mean = 3.7), than question 2, 4, 6, 7, and 8 that related to intrinsic transistor model parameters and dominant poles (mean = 2.9). Each of these two general categories experience an overall average confidence gain: +1.4 for the transistor amplifier design questions and +1.0 for the questions related to intrinsic transistor model parameters and dominant poles.

V. Summary

The development of a meaningful student laboratory experience in transistor amplifier design with the a closed loop approach for finding intrinsic transistor capacitor values using SPICE and circuit analysis met its goals. Good correspondence between simulation results and model parameter calculations were achieved.

A method to accurately determine the transistor intrinsic capacitances was developed and demonstrated. The accurate correspondence of simulation, analysis and experimental enhances student confidence in the learning process.

Acknowledgement
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IV. Bibliography

1. D. Costa, W. U. Liu, and J. ***S.*** Harris **Jr.,** "Direct extraction of the AIGaAs/GaAs heterojunction bipolar transistor small-signal equivalent circuit," ***IEEE Trans. Electron Devices,*** vol. 38, **pp.** 201 8-2024, Sept. 1991.
2. I. E. Getreu, ***Modeling the Bipolar Transistor.*** Amsterdam: Elsevier, 1978
3. Thomas F. Schubert,, Jr. and Ernest M. Kim, A Short Study on the Validity of Miller's Theorem Applied to Transistor Amplifier High-Frequency Performance" IEEE Transactions on Education, vol. 52, no. 1 pp. 92-98, February 2009.
4. Thomas F. Schubert,, Jr., Frank G. Jacobitz, and Ernest M. Kim, "The Engineering Design Process: An Assessment of Student Perceptions and Learning at the Freshmen Level", *Proceedings of the 2009 ASEE Annual Conference & Exposition,* Austin, TX, June 14-17, CD-ROM, 2009
5. Thomas F. Schubert,, Jr., Frank G. Jacobitz, and Ernest M. Kim, "Exploring Three-Phase Systems and Synchronous Motors: A Low-Voltage and Low-Cost Experiment at the Sophomore Level", IEEE Transactions on Education, pp. 67-76, vol. 54, no. 1, February 2, 2011.