ASEE AMERICAN SOCIETY FOR ENGINEERING EDUCATION

Paper ID #27802

Research Experience for Community College Students: Design and Optimization of Non-Volatile Latch using Anti-Fuse Memory Technology

Mr. Michael Gee, Canada College

I'm a third year Mechanical Engineer major at Canada Community College and I plan to transfer to a CSU or UC in the Fall of 2019.

Anthony Akash Lal
Alex E Hercules
Tyler Sheaves, San Francisco State University

A graduate researcher at San Francisco State University's Nano Electronics and Computing Research Lab (NeCRL). He has assisted in multiple projects involving hardware and IP security, typically focusing research efforts on development and automation of complex integrated circuit workflows and low-level device architecture. Each Summer since joining NeCRL, he has assisted in the ASPIRES Summer bridge program which aims to assist first-generation college students, in underrepresented groups, studying STEM fields, transition from community colleges into research roles at four-year universities. Tyler has been a researcher at NeCRL since 2016 and will be graduating with a Masters in Embedded Electrical and Computer Systems in Fall of 2019.

Dr. Amelito G Enriquez, Canada College

Amelito Enriquez is a professor of Engineering and Mathematics at Cañada College in Redwood City, CA. He received a BS in Geodetic Engineering from the University of the Philippines, his MS in Geodetic Science from the Ohio State University, and his PhD in Mechanical Engineering from the University of California, Irvine. His research interests include technology-enhanced instruction and increasing the representation of female, minority and other underrepresented groups in mathematics, science and engineering.

Dr. Cheng Chen, San Francisco State University

Dr. Cheng Chen is currently an associate professor in the school of engineering at San Francisco State University. His research interests include earthquake engineering, structural reliability and fire structural engineering.

Dr. Hao Jiang, San Francisco State University

Hao Jiang received the B.S. degree in materials sciences from Tsinghua University, China, in 1994 and the Ph.D. degree in electrical engineering from the University of California, San Diego, in 2000.

Hao Jiang has been with San Francisco State University since August 2007 as an assistant professor in electrical engineering. Prior joining SFSU, he worked for Broadcom Corporation, Jazz Semiconductor and Conexant Systems Inc. His research interests are in the general area of analog integrated circuits, particularly in ultra-low-power circuits for biomedical applications.

Dr. Zhaoshuo Jiang P.E., San Francisco State University

Zhaoshuo Jiang graduated from the University of Connecticut with a Ph.D. degree in Civil Engineering. Before joining San Francisco State University as an assistant professor, he worked as a structural engineering professional at Skidmore, Owings & Merrill (SOM) LLP. As a licensed professional engineer in the states of Connecticut and California, Dr. Jiang has been involved in the design of a variety of low-rise and high-rise projects. His current research interests mainly focus on Smart Structures Technology, Structural Control and Health Monitoring and Innovative Engineering Education.

Dr. Wenshen Pong P.E., San Francisco State University

Wenshen Pong received his Ph.D. in Structural Engineering from the State University of New York at Buffalo. He joined the School of Engineering at San Francisco State University in 1998. He teaches courses in Civil/Structural Engineering.

Dr. Pong is a registered Professional Engineer in California. He is a member of the American Society of Civil Engineers and the Structural Engineers Association of California. He has published over fifty technical papers in the areas of Structural Control and Earthquake Engineering. Dr. Pong was the Director of the School of Engineering at SFSU with 20 full-time faculty and over 25 part-time faculty from 2009 to 2018.

Dr. Xiaorong Zhang, San Francisco State University

Xiaorong Zhang received the B.S. degree in computer science from Huazhong University of Science and Technology, China, in 2006, the M.S. and the Ph.D. degrees in computer engineering from University of Rhode Island, Kingston, in 2009 and 2013 respectively. She is currently an Assistant Professor in the School of Engineering at San Francisco State University. Her research interests include embedded systems, wearable technologies, neural-machine interface, and cyber-physical systems.

Prof. Hamid Mahmoodi, San Francisco State University

Hamid Mahmoodi received his Ph.D. degree in electrical and computer engineering from Purdue University, West Lafayette, IN, in 2005. He is currently a professor of electrical and computer engineering in the School of Engineering at San Francisco State University. His research interests include low-power, reliable, and high-performance circuit design in nano-electronic technologies. He has published more than one hundred technical papers in journals and conferences and holds five U.S. patents. He was a co-recipient of the 2008 SRC Inventor Recognition Award, the 2006 IEEE Circuits and Systems Society VLSI Transactions Best Paper Award, 2005 SRC Technical Excellence Award, and the Best Paper Award of the 2004 International Conference on Computer Design. He has served on technical program committees of Custom Integrated Circuits Conference, International Symposium on Low Power Electronics Design, and International Symposium on Quality Electronics Design.

Research Experience for Community College Students: Design and Optimization of Non-Volatile Latch using Anti-Fuse Memory Technology

Michael Gee[1], Anthony Akash Lal[1], Alex Hercules[1], Tyler Sheaves[2], Amelito G. Enriquez[1], Cheng Chen[2], Hao Jiang[2], Zhaoshuo Jiang[2], Wenshen Pong[2], Hamid Shanasser[2], Kwok-Siong Teh[2], Xiaorong Zhang[2], Hamid Mahmoodi[2]

[1]Canada College, Redwood City, CA
[2]San Francisco State University, Daly City, CA

Abstract

A ten-week summer research internship program is designed and implemented for community college students. The research activity is performed in a four-year university under the guidance of a faculty in charge of the research program, and the research interns are assigned a graduate student mentor. The results of this program include research experience given to the community college students early in their educational pathways. Such early exposure to research has benefits of improved students' outlooks which improve their performance in their coursework and sharpen their interest in pursuing STEM fields. Given the often-lengthy background preparation needed for conducting research, it is difficult to incorporate research experience as a curricular activity in regular semesters when students have a lot of distractions managing various assignments in different courses. Summer is a time when students have fewer distractions and can be effectively engaged in a focused research activity. The intern cohort are divided to discipline of Electrical, Computer, Mechanical, and Civil Engineering. This paper presents the details of the project for the Electrical Engineering cohort, the research, and educational objectives, results obtained. The planned research project for the Electrical cohort is related to anti-fuse memory technology, which is a promising one-time programmable nano-scale technology for information storage. In this technology, the information is stored in a resistive form which is a state of a fuse element that is non-volatile. In this research, we propose a unique application for anti-fuse memory technology and that is to realize non-volatile single-bit latch element that can be used for building re configurable logic circuits. The entire intern cohort are surveyed at the end of the program to assesses the program outcomes. According to the student surveys, the results suggest that research experience is very valuable in encouraging students to pursue STEM research careers. Moreover, this experience enhances students' technical research skills such as scientific thinking, ability to analyze and interpret results, and presentation skills. This flipped approach to educational pathways in which research experience is offered early on results in students to be more determined and motivated as they progress through their educational pathways.

1. Introduction

Background: With funding from the Department of Education, Canada community college and San Francisco Sate University have collaborated to offer research internship experience to the under-represented community college students. This program has been conducted for several years

now and every year it impacts close to 20 community college students. The community college students are selected for this program based on criteria of diversity, technical background, and fit. The program covers four disciplines of Electrical, Computer, Mechanical, and Civil Engineering. In each discipline, there is a faculty research advisor at San Francisco State University who is in charge of defining the research plan and hosting the inters in his/her research laboratory over the summer and providing a graduate student mentor.

The paper presents the activity planned for the Electrical Engineering cohort and its results for offering research experience to the undergraduate students to inspire them to pursue higher education and research careers. An effective research experience for undergraduate students requires proper definition of a focused research problem, proper training and mentoring. In Summer 2018, we have been able to host three undergraduate students as the Electrical Engineering cohort from the community college in our research laboratory in the 4-year university. The undergraduate student research interns were mentored by a master student who was experienced in the assigned research topic. A dedicated faculty member oversaw defining and supervising the research tasks.

The research internship was conducted for ten weeks during summer. Undergraduate student interns had weekly meetings with their mentor and faculty advisor. The assigned research task was to explore design optimizations for a Non-Volatile Latch (NV-Latch) memory element using anti-fuse memory technology. The research tried to evaluate the influence of various transistor sizing on area and power and performance trade-offs in the design. Overall, the end design goal was to construct an optimal design which could achieve the best performance and reliability under a given silicon area budget. Throughout the introductory phase, students were given orientation and resources to learn the basics of the technology under investigation and the operation of the NV-latch module. They were also given tutorials to learn the spice circuit modeling and simulation. Students were tasked to collect power, performance, and area results of various design points. After data collection, students were then asked to interpret the results and offer meaningful conclusions as to the design optimization process and results achieved.

Throughout the program, students made midterm and final project progress report in both written and oral presentation forms to practice their writing as well as oral presentation skills. The students were surveyed on the effectiveness and satisfaction of their research experience before exiting the program.

Objective: The objective of this research internship program was to offer diverse and underrepresented community college students an early exposure to research in STEM fields in order to improve their interest and performance in the STEM fields. This objective is assessed by surveying the intern using the same questionnaire at the beginning and at the end of this program and measuring the difference in their responses.

This paper shares the research project details, research results, and the student survey results. Section 2 presents a brief literature review of relate work and best practices in offering research internship to students. Sections 3 through 6 of the paper are about the research work the students conducted and may not be directly relevant to the education theme, but they represent a sample of the writing the student prepared at the end of the internship.

2. Literature Review and Best Practices

There are many works published on research internship as a vehicle for improving engineering education [4-11]. The target population for research internship varies from high school students [4], to undergraduate students [5], graduate students [6], and faculty [7]. A common observation in all these works is that internship experience does improve the educational outcome for the participants. When it is targeted for high school students, it can assist in increasing diversity in STEM disciplines by encouraging female and minority students to choose STEM fields for their college [4]. When internship is offered to lower division undergraduate students, it improves their retention in the STEM fields [5]. When offered to graduate students, it results in improved research quality [6]. When offered to faculty member, it assists faculty in maintaining currency in knowledge and skills [7]. The research and internship activities for undergraduate students have been shown to improve their retention and learning abilities in their classroom educational activities [11]. The scalability of offering research and internship opportunities to mass number of undergraduate students remains to be a challenge.

3. Research Project Background: Anti-Fuse Memory Technology

The anti-fuse device is a cell whose insulating element breaks down under a high electric field, which is made of transistor-dielectric or metallic materials. Anti-fuses are manufactured as high resistance devices whose resistance can be permanently altered to a low resistance value by placing a sufficient electric field across it. Once programmed the resistance value cannot be reversed, hence an anti-fuse is one-time programmable. These devices may also be either fabricated at a metal layer above the transistors of our design at no area cost or may occupy a small area (Fig. 1). For metal-to-metal based anti-fuses depicted in Figure 1, the high electric field results in permanent conductive paths being formed between initially isolated regions of metal layers (Fig. 2). Other types of programmable anti-fuses exist, but for the purposes of this paper we will assume a metal-to-metal type cell which can be fabricated above our transistor array, and, therefore, shows a lower bit-cell area.

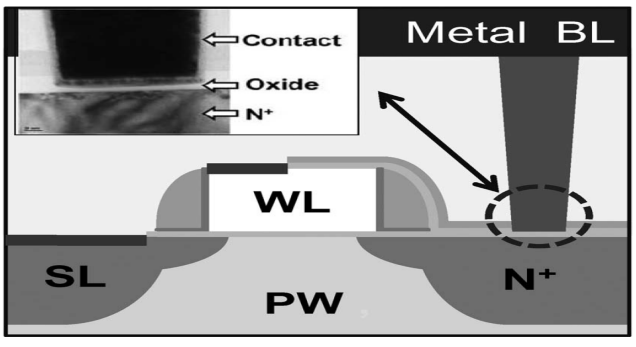

Figure 1. Programmable-Contact Based Anti-Fuse [Chen, 2009]

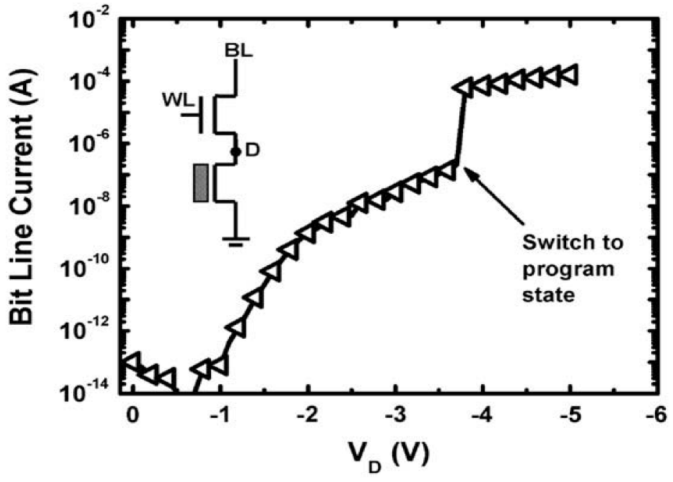

Figure 2. Example of Programming of 45nm Anti-fuse [Tsai, 2009]

4. Research Project Task: Design a Non-Volatile Latch using Anti-Fuse Memory Technology

The latch is the most fundamental unit of binary data storage. A Non-Volatile (NV) latch is a type that does not lose its binary state when the power supply is lost. The use of non-volatile latches includes storage of identification numbers such as serial numbers, secret key, configuration bits, etc.

A typical non-volatile latch must have the ability to be programmed to a binary state and retain this binary state even in the case of power down. The state of the latch can be queried by other components as long as system power is present. Looking at **Figure 3**, a basic latch can have control inputs for reading or sensing the stored data ('SE'), a data input ('D') whose state is stored to the latch, and an output which presents its current binary state (referred to as 'Q'). By storing the state of the latch in the anti-fuse element, that data is stored permanently in a non-volatile form. An additional programming control input write enable ('WE') is needed to activate the programming of the internal fuse element. The research task is to design and optimize this non-violate anti-fuse based latch in a 28 nm CMOS technology.

***Figure 3**. Block-Level NV Latch I/O*

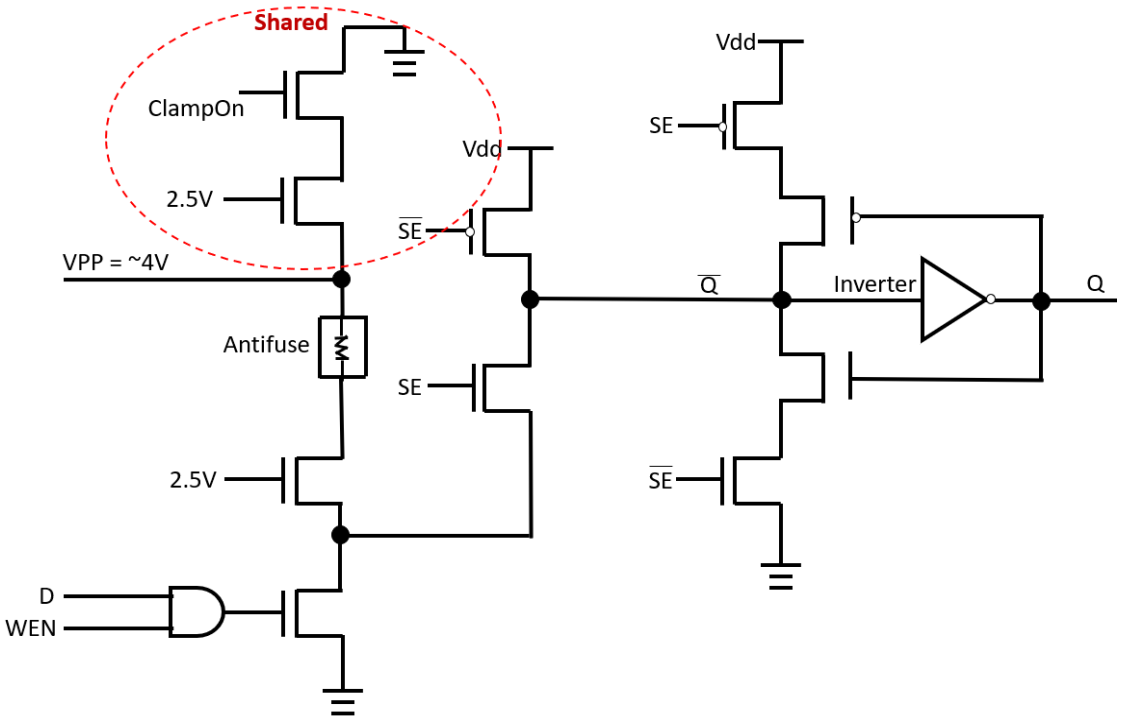

Figure 4. *Proposed Design of Anti-Fuse Based NV Latch*

Figure 4 provides a transistor-level view of the proposed anti-fuse-based latch, which is to be designed in a 28 nm generic process development kit (PDK). VPP is the fuse programming voltage which will provide the necessary electric field, this signal will be set to a reported DC value of 4-5 Volts during a write operation. All 2.5V gate-input transistors are always on and serve as protection for core transistors whose maximum rated voltage is 1.05V at the 28 nm technology node. The 'Clamp-On' signal serves as the circuit's connection to ground during read operations. 'Clamp-On' is off during write to ensure the only DC path to ground is through the anti-fuse device depending on the data input ('D') and is on during read operation. 'D' is the circuit's data input and acts as the user's input to the circuit allowing the user to either apply an electric field potential of 'VPP' or 0 across the anti-fuse. The signal 'WE' is the write enable signal which will allow the data input to either alter the potential across the anti-fuse or stop any potential from being applied. The 'SE' signal corresponds to the device's sense enable (read) function. When this signal is high, and if write enable is low, the latch will convert the resistive state of the anti-fuse to a voltage value at output 'Q'. It is important to note that everything above the anti-fuse element is shared across all anti-fuse cells on-chip, which means that the total unit-cell consists of just 16 transistors (only 3 of which are non-minimum size) and an anti-fuse element which may be manufactured on top of the latch (meaning no additional area cost).

5. Anti-Fuse-Based NV Latch Optimization

The design needs to be optimized in order to function with a low expected rate of failure. The following general approach was followed for this optimization:

1. **Identify transistors which might impact read/write reliability perform parametric sweeps with delay-based Monte Carlo simulations [1] at every parametric test to identify trends in reliability.**
2. **Select sizing of transistors such that pre-layout failure rates are no more than 0+-.001%.**
3. **Perform Layout.**
4. **Re-simulate Monte Carlo analysis and re-size transistors if necessary.**
5. **Characterize bit-cell.**

All simulations were carried out using a collection of Synopsys tools CDESIGNER, Hercules, IC Validator, and HSPICE.

The Anti-fuse latch is susceptible to read failures due to its single-ended design. A voltage divider is formed during the sensing of a low resistive state. If the PMOS with input SEb is not sized properly sensing failure would occur. Also, since a high voltage (VPP) is present on-chip, specific high voltage transistors need to be monitored to ensure no transistors gate-to-source, gate-to-drain, or source-to-drain voltage exceed its rated voltage. Finally, a sufficient electric field or voltage (at least 4 Volts) need to be present across the anti-fuse device during write. Therefore, the Monte Carlo failure conditions are defined as follows:

1. **Sensing failure during Anti-fuse read cycles resulting in mis-read output 'Q'**. The Anti-fuse may have too large of a low-resistance to evaluate to a proper high output. To mitigate this, we create a larger resistance on the PMOS-type transistor with an input of 'SEb'
2. **Voltage/Current across the Anti-fuse insufficient.** The Anti-fuse itself has specific write current and device voltage needed to achieve a change in resistive state. If these are not met the device cannot be written to properly.

Due to a lack of available robust models, the Anti-fuse was modeled at its measured blown and unblown resistance and capacitive values reported in the literature. A blown resistance is reported to be 15 kOhms, an unblown resistance of 15 MOhms (a ratio of 10^5) and a parasitic unblown capacitance of 5 fF [2-3]. A failed Monte Carlo iteration can be detected by a gate-drain, gate-source or source-drain voltage exceeding 10% of our 2.5V rated shielding transistors, by a false 'Q' or 'Qb' reported after sensing (see Figure 5 for example), or by insufficient write current (less than 20uA).

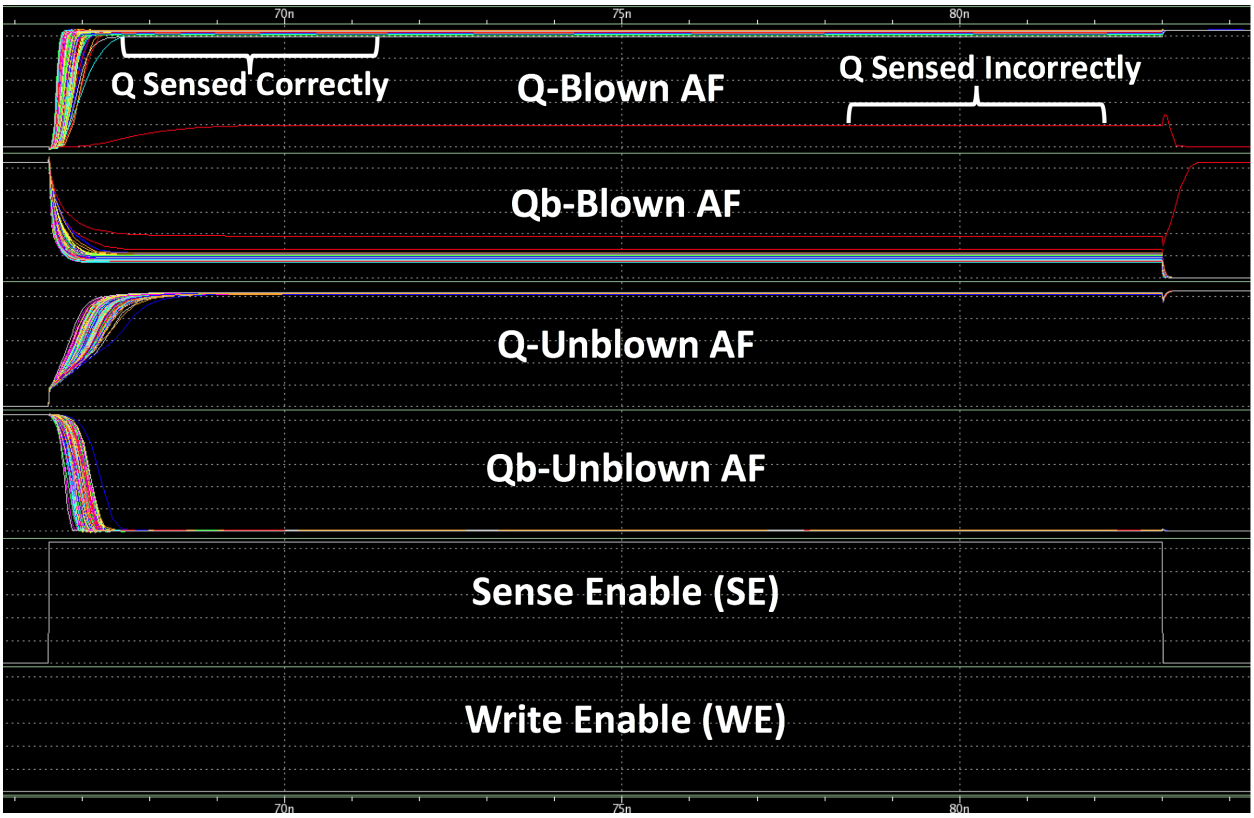

Figure 5. Anti-Fuse Monte Carlo Results Depicting a Sensing Error

6. Anti-Fuse NV-Latch Results

Due to a lack of a robust model many failure criteria were necessary which are listed as additional metrics in Table 1. Histograms of optimized post-layout measurements shown in Figures 6 through 8 displays all criteria were met at the target reliability. Finally, Figure 9 shows the layout of the Anti-fuse bit-cell.

Anti-Fuse Reliability Metric Failure Criteria		
Max Gate-to-Source Voltage +/-	2.75	Volts
Max Gate-to-Drain Voltage +/-	2.75	Volts
Max Drain-to-Source Voltage +/-	2.75	Volts
Min AF Unblown Write Current	50	Micro-Amps
Min Program Voltage Unblown AF	3.6	Volts
Min Q Blown	0.945	Volts
Max Qb Blown	0.105	Volts
Max Q Unblown	0.105	Volts
Max Qb Unblown	0.945	Volts
Anti-Fuse-Based Latch Characteristics Post-Optimization		
Static Power Pre-Layout	43.863	Nano-Watts
Static Power Post-Layout	70.3817	Nano-Watts
Sense-Delay Pre-Layout	15.8751	Pico-Seconds
Sense-Delay Post-Layout	933.136	Pico-Seconds
Reliability Achieved	100±.001%	Percent
Cell Area	7.733	Micro-Meters^2
Write Delay (Reported)	20	Micro-Seconds
Write Current (Reported)	50	Micro-Amps
Resistive Ratio (Reported)	10^5	High/Low
Optimized SRAM-Based Latch Reference Characteristics		
Static Power Pre-Layout	N/A	Nano-Watts
Static Power Post-Layout	140.8	Nano-Watts
Sense-Delay Pre-Layout	N/A	N/A
Sense-Delay Post-Layout	N/A	N/A
Reliability Achieved	Standard Cell	Percent
Cell Area	6.61	Micro-Meters^2
Write Delay (Reported)	3.12	Nano-Seconds
Write Current (Reported)	370	Nano-Amps
Resistive Ratio (Reported)	N/A	N/A

Table 1. *Optimized Anti-fuse Failure Criteria, Final Design Metrics, And DFF Reference Comparison*

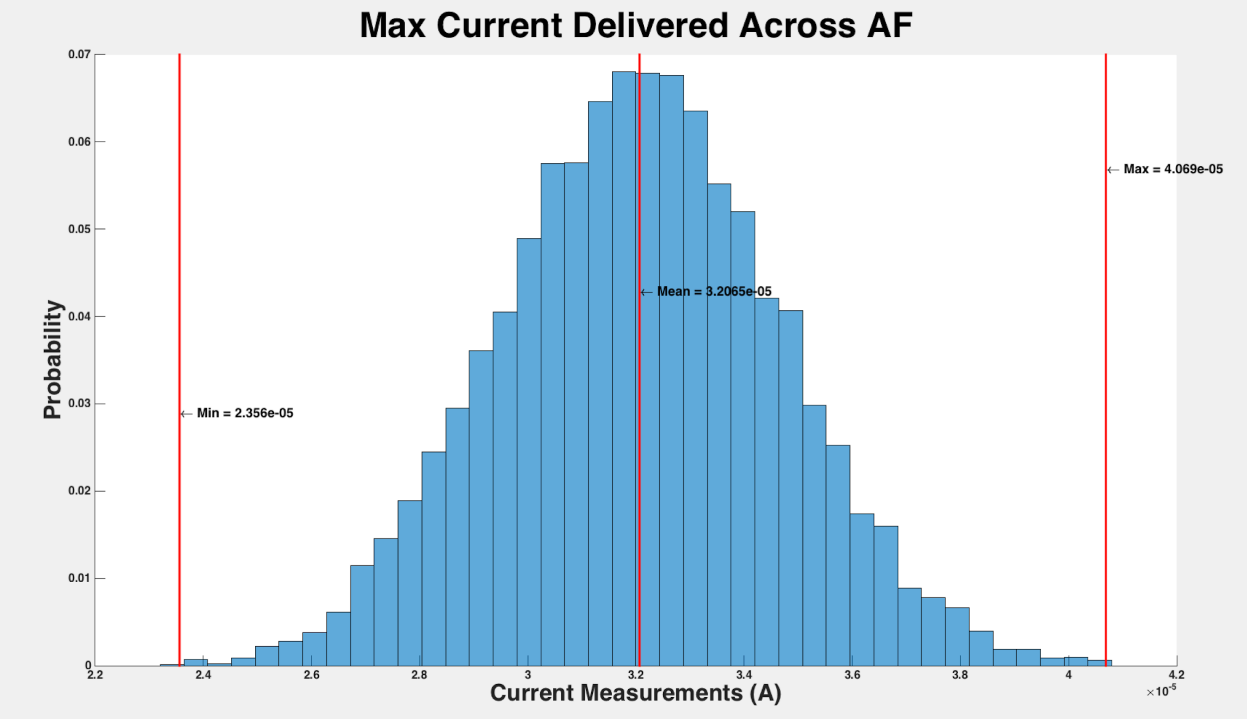

Figure 6. *Max current delivered across Anti-fuse*

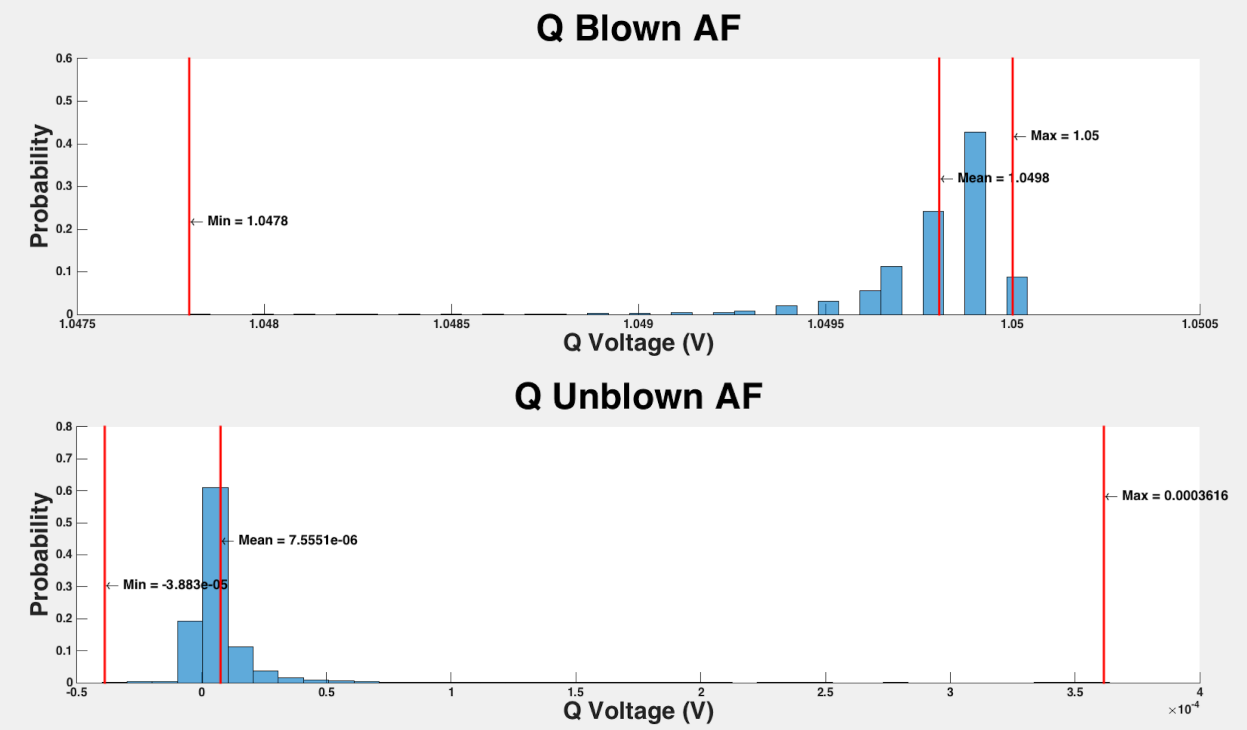

***Figure 7**. Anti-fuse Blown and Unblown voltages for Q*

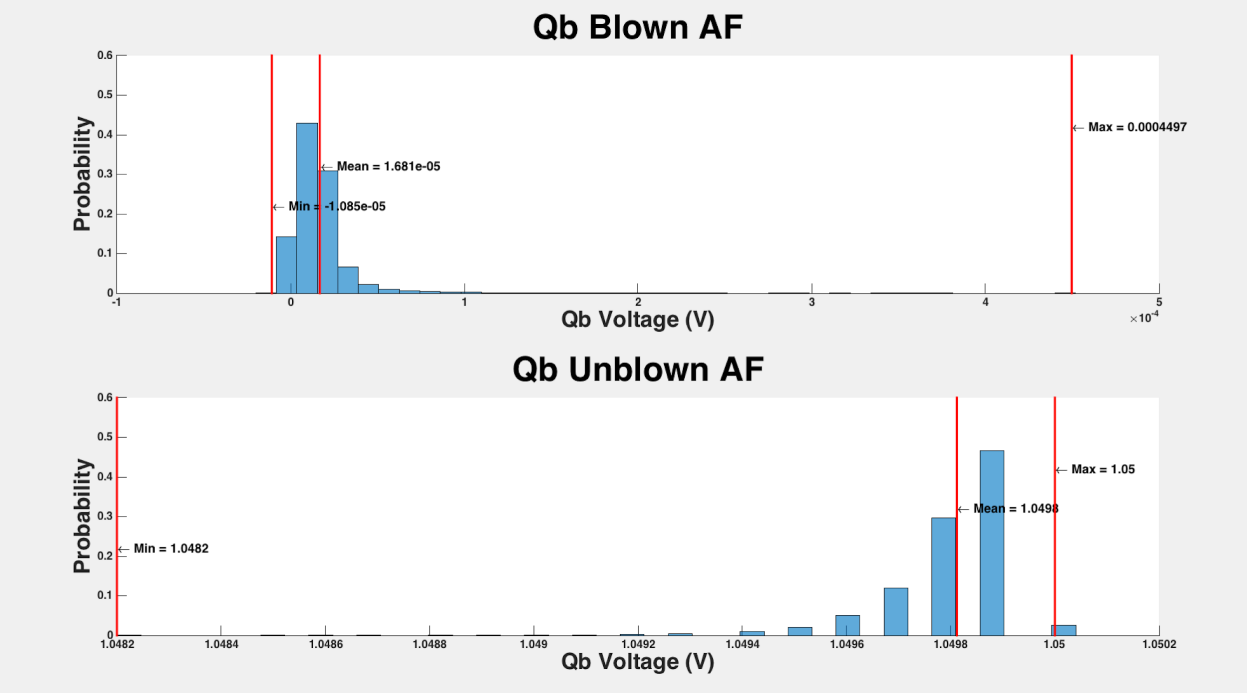

***Figure 8**. Anti-fuse Blown and Unblown voltages for Qb*

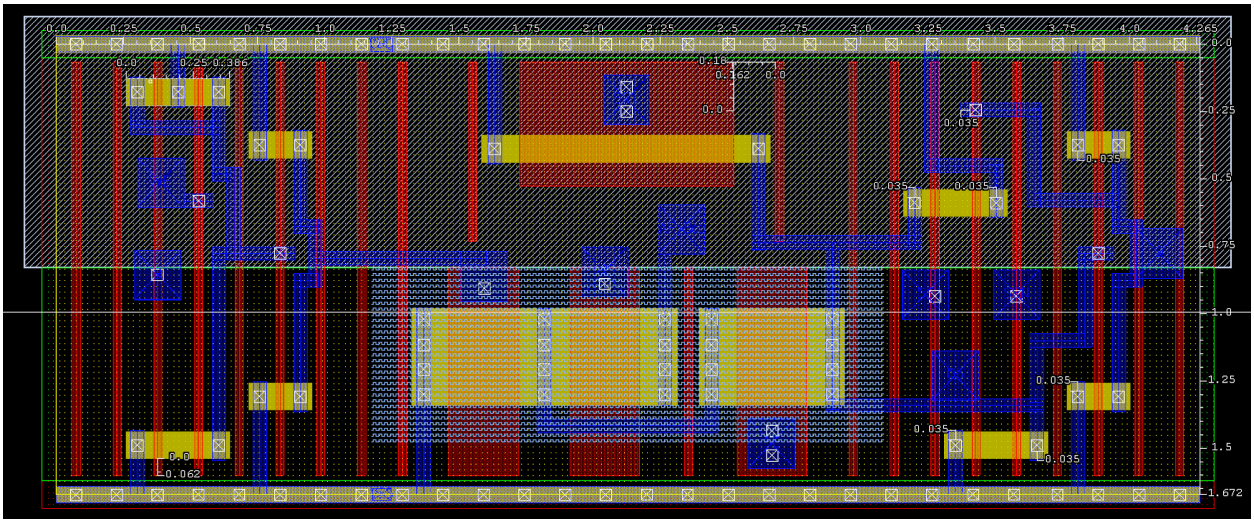

Figure 9*. Anti-fuse Based NV Latch Layout*

7. Student Surveys

Surveys were conducted on the entire cohort of research interns from all disciplines of Electrical, Computer, Mechanical, and Civil Engineering. There were close to 20 interns who were surveyed. Table 2, 3 and 4 summarize the results of pre- and post-program student surveys designed to measure perception and overall impact of the research internship program on student participants. From Table 1, it is observed that while generally students had high level of agreements to all questions asked on the purpose of doing a research internship, they noticeably showed a higher level of confidence in choosing a STEM research career after the internship. This shows that doing a research internship offers students a better insight into nature of STEM fields so that they can better decide if they want to pursue STEM research.

Table 2 shows that the participant had a high level of satisfaction with different parts of the internship program. Table 3 shows the improvements in technical skills obtained by students going through the internship program. Most notably students' understanding of a scientific approach to real problems improved significantly. Students also showed improvements in understanding the research process, integrating theory and practice, analyzing data and other information, giving an effective oral presentation, and scientific writing.

Table 2. Survey on Purpose of internship. *1 - Strongly Disagree and 5 –Strongly Agree.*

	Post	Pre	Diff
gain hands-on experience in research	4.28	4.72	-0.44*
solidify my choice of major	3.92		
gain skills needed to successfully complete a BS degree	4.12		
clarify whether graduate school would be a good choice for me	4.08	4.08	0.00
clarify whether I wanted to pursue a STEM research career	4.08	3.84	0.24
work more closely with a particular faculty member	4.00	4	0.00

get good letters of recommendation	3.80	4.08	-0.28
have a good intellectual challenge	4.28	4.48	-0.20
read and understand a scientific report	4.24		
write a scientific report	4.00		
ask good questions related to the scientific process	4.20		
set up a scientific experiment	4.16		
work with others to plan and conduct scientific experiments	3.96		
talk to professors about science	4.04		
think like a scientist	4.12		

* The change is statistically significant at $p < 0.050$.

Table 3. How satisfied are you with each of the following? 1 being LEAST satisfied and 5 being MOST satisfied.

Opening Day at SFSU (June 6th)	4.43
Faculty Adviser Description of Project (June 6th)	4.39
Meetings with Graduate Student Mentor	4.40
Meetings with Faculty Adviser	4.21
Mid-Program Presentations (July 21st)	4.48
Final Presentations (August 12th)	4.27
The results of your project	4.12
Your final poster	4.38
Your final presentation	4.33
How much you learned from the program	4.60
Your group mates	4.17
Your faculty adviser	4.46
The Summer Internship Program as a whole	4.48

Table 4. Please indicate your level of agreement with the following statements.
1-Strongly Agree, 5-Strongly Agree.

Prompt	**Post**	**Pre**	**Diff**
I was able to conduct the scientific research that is part of my summer internship.	4.48		
I am confident I will transfer to a four-year institution.	4.76	4.80	-0.04
I am confident I will complete a BS in a STEM field.	4.64	4.72	-0.08
I can imagine myself continuing after my BS to pursue a Master's Degree in a STEM field .	4.32	4.24	0.08
I can imagine myself continuing after my BS to pursue a Ph.d. in a STEM field/Medical School/other education beyond the Master's level.	3.88	3.60	0.28
I have a clear career path.	4.28	4.04	0.24
I have skill in interpreting results.	4.28	3.96	0.32
I have tolerance for obstacles faced in the research process.	4.40	4.12	0.28
I am ready for more demanding research.	4.28	3.88	0.40
I understand how knowledge is constructed.	4.32	3.96	0.36
I understand the research process in my field.	4.28	3.56	0.72**

I have the ability to integrate theory and practice.	4.20	3.84	0.36
I understand how scientists work on real problems.	4.40	3.52	0.88**
I understand that scientific assertions require supporting evidence.	4.52	4.04	0.48*
I have the ability to analyze data and other information.	4.40	4.04	0.36
I understand science.	4.36	3.88	0.48*
I have learned about ethical conduct in my field.	3.96	3.96	0.00
I have learned laboratory techniques.	4.32	4.00	0.32
I have an ability to read and understand primary literature.	4.40	4.00	0.40
I have skill in how to give an effective oral presentation.	4.40	4.04	0.36
I have skill in science writing.	4.08	3.68	0.40
I have self-confidence.	4.32	4.08	0.24
I understand how scientists think.	4.24	3.84	0.40
I have the ability to work independently.	4.64	4.16	0.48*
I am part of a learning community.	4.16	4.36	-0.20
I have a clear understanding of the career opportunities in science.	4.24	4.16	0.08

* The change is statistically significant at $p < 0.050$.
** The change is statistically significant at $p < 0.010$.

8. Conclusion

We developed a summer research internship program in which three undergraduate students from a community college were involved in a research program in a 4-year university in the area of non-volatile latch design using anti-fuse technology. The student interns were mentored by a graduate student and supervised by a dedicated faculty member in charge of the research project. The student interns were tasked to perform design optimizations on a non-volatile latch designed using anti-fuse technology. The students also prepared written and oral presentation on their research findings. The student interns were surveyed at the end of the program to measure their satisfaction with the offered research experience and the impact on their educational and career perspective. The survey confirmed that the participants formed a higher level of confidence in pursuing STEM careers after participating in this program. The scalability of this program to reach to a border student body is a challenge.

9. Bibliography

[1] Wicht, Bernhard, Thomas Nirschl, and Doris Schmitt-Landsiedel. "Yield and Speed Optimization of a Latch-Type Voltage Sense Amplifier." IEEE JOURNAL OF SOLID-STATE CIRCUITS , VOL.39 NO.07, JULY 2004

[2] E. R. Hsieh *et al*., "The demonstration of low-cost and logic process fully-compatible OTP memory on advanced HKMG CMOS with a newly found dielectric fuse breakdown," *2015 IEEE International Electron Devices Meeting (IEDM)*, Washington, DC, 2015, pp. 3.4.1-3.4.4.

[3] M. Deloge, B. Allard, P. Candelier, J. Damiens, E. Le-Roux and M. Rafik, "Application of a TDDB Model to the Optimization of the Programming Voltage and Dimensions of Antifuse Bitcells," in *IEEE Electron Device Letters*, vol. 32, no. 8, pp. 1041-1043, Aug. 2011.

[4] Genalo, L. (2003, June), *Summer Industry Based Research Internships For Female High School Students* Paper presented at 2003 Annual Conference, Nashville, Tennessee. https://peer.asee.org/11606

[5] Seevers, M., & Pyke, P., & Knowlton, W., & Schrader, C., & Gardner, J. (2006, June), *Improving Engineering Undergraduate Retention Via Research And Internships* Paper presented at 2006 Annual Conference & Exposition, Chicago, Illinois. https://peer.asee.org/1394

[6] Baez-Rivera, Y., & Brown, L., & Schulz, N. (2007, June), *Using Graduate Internships To Enhance Graduate Student Education And Research* Paper presented at 2007 Annual Conference & Exposition, Honolulu, Hawaii. https://peer.asee.org/2398

[7] Griffin, J. A., & Homkes, R. L. (1999, June), *Faculty Internships* Paper presented at 1999 Annual Conference, Charlotte, North Carolina. https://peer.asee.org/7670

[8] Schmidt, J. (2003, June), *Rise: Research Internships In Science And Engineering* Paper presented at 2003 Annual Conference, Nashville, Tennessee. https://peer.asee.org/12439

[9] Fowinkle, L. (2018, August), *Internship Opportunities for Millennial Students* Paper presented at 2018 ASEE Conferences - Conference for Industry and Education Collaboration / San Antonio proceedings, San Antonio. https://peer.asee.org/31357

[10] Pearson Weatherton, Y., & Chen, V. C. P., & Mattingly, S. P., & Rogers, K., & Sattler, M. L. (2012, June), *Sustainable Engineering Internships: Creation and Assessment* Paper presented at 2012 ASEE Annual Conference & Exposition, San Antonio, Texas. https://peer.asee.org/21976

[11] Powers, K., & Chen, H. L., & Prasad, K. V., & Gilmartin, S. K., & Sheppard, S. (2018, June), *Exploring How Engineering Internships and Undergraduate Research Experiences Inform and Influence College Students' Career Decisions and Future Plans* Paper presented at 2018 ASEE Annual Conference & Exposition , Salt Lake City, Utah. https://peer.asee.org/30491